LOADSLAMMER
TRUST AND VERIFY

PactivR Data Sheet

Features

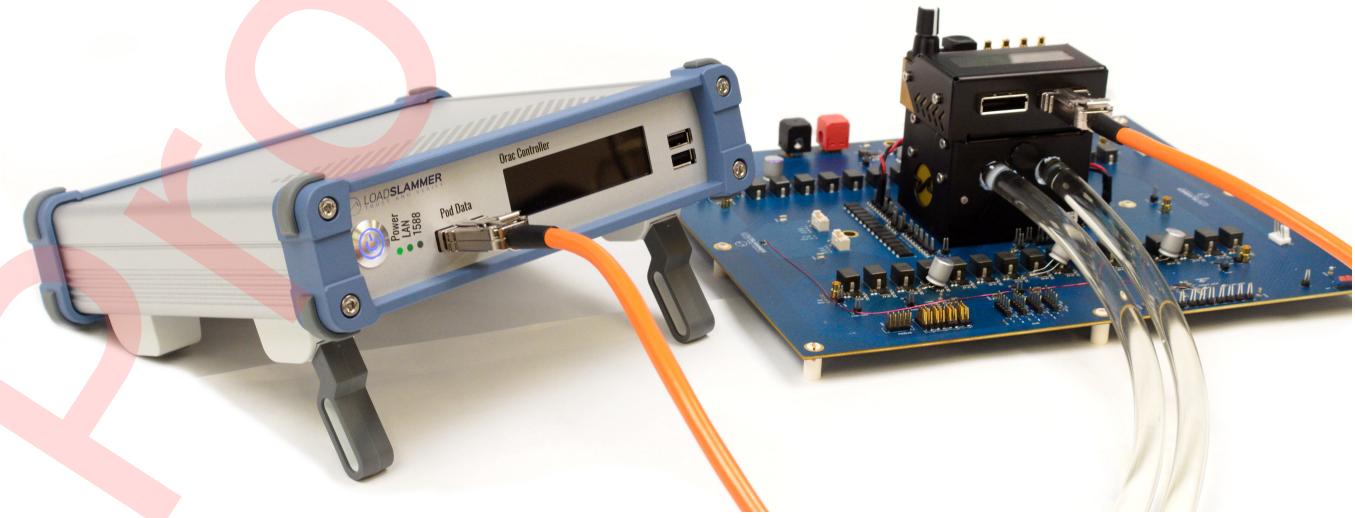
- 30 Software Configurable 60A LoadCell Array
- 20 Differential Voltage sense pairs
- 16 GPIO to interact with system
- PMBus + AVS Bus support
- Up to 1500W Continuous

General Description

The PactivR Power System Test Tool closes the loop on power systems testing. Speed up your development cycles and time to market using the automated test suite provided by the Orac platform. Automated test pattern generation, testing, analysis, and tuning for your power system.

Applications

- CPU, GPU platforms
- ASIC Development
- AI/ML Processors
- Embedded System Development
- Edge Compute System Development



Electrical Specifications

All specifications are in $0°C \leq T_A \leq 45°C$ unless otherwise noted.

Table 1: LoadCell Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Passive						
Minimum LoadCell resistance	R_{min}		10		mOhm	Standard SKU
	R_{min}		18		mOhm	High-Voltage SKU
M-F Socket resistance	R		2		mOhm	per LoadCell
F-M-F Socket resistance	R		4		mOhm	per LoadCell
LoadCell inductance	L	360	480	600	pH	
M-F Socket inductance	L		180		pH	per LoadCell
F-M-F inductance	L		250		pH	per LoadCell
Static						
Input Voltage	V_{max}		30		V	Standard SKU
	V_{max}		80		V	High-Voltage SKU
Maximum instantaneous current	$I_{max(inst.)}$		60		A	Standard SKU
	$I_{max(inst.)}$		15		A	High-Voltage SKU
Maximum continuous current	$I_{max(cont.)}$		30		A	Standard SKU
	$I_{max(cont.)}$		12		A	High-Voltage SKU
Maximum instantaneous power	$P_{max(inst.)}$		100		W	
Maximum continuous power	$P_{max(cont.)}$		50		W	
Dynamic						
Edge time	t_{edge}	24			ns	

Table 2: PMBus Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Pull-up voltage	V_{pullup}	1.2		3.3	V	
Dynamic						
Clock frequency	f_{max}	100		400	kHz	

Table 3: GPIO Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
HIGH-level input voltage	V_{IH}	2.31		5.5	V	
LOW-level input voltage	V_{IL}	-0.5		1.0	V	
HIGH-level output voltage	V_{OH}	2.7			V	I_{OH} = -8 mA
LOW-level output voltage	V_{OL}	0.25			V	I_{OL} = 8 mA
Dynamic						
Maximum toggle rate	f_{toggle_max}			1	kHz	

Table 4: User FPGA Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Supply voltage for IO	V_{CCIO}[1]	1		3.3	V	

[1] All V_{CCIO} must be powered up to use the User FPGA. Can be left unconnected if unused.

Table 5: External I/O Electrical Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Differential High-Voltage Sense Inputs (EXT1, EXT2)						
Maximum voltage	V_{max}		$\pm$ 60		V	
Differential DC Meter Sense (EXT1, EXT2, EXT3, EXT4)						
Maximum voltage	V_{max}		$\pm$ 60		V	
Sample Rate	f_{sample_rate}		128		kSPS	
Bit-depth			24		bits	
Differential Monitor Outputs						
Output common mode voltage	V_{ocm}		0		V	
Output voltage swing	V_{swing}	-4		4	V	

Thermal Specifications

Table 6: Thermal Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
LoadCell thermal resistance	θ_{JL}		3.6		°C/W	Junction to liquid
LoadCell maximum junction temperature	T_{max}		150		°C	
Maximum liquid coolant temperature	T_{lqiud}			50	°C	
Ambient operating temperature	T_A			45	°C	

Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

Parameter	Rating
External I/O voltage	±100 V
LoadCell input voltage	40 V (Standard SKU) 100 V (High-Voltage SKU)
Socket voltage sense input	±5 V
GPIO MIN voltage	-0.6 V
GPIO MAX voltage	5.5 V
GPIO output current (total)	±20 mA
User FPGA VCCIO (UIO_PWR_y)	3.9 V
Storage temperature	60 °C

Note: Stresses above those listed under Absolute Maximum Ratings can cause permanent damage to the device. This is a stress rating only. Functional operation of the device is not implied in any conditions above those indicated in the Electrical Specifications section.

Socket

There are multiple options for connecting the PactivR to a DUT depending on your specific use cases and needs. Please contact ProGrAnalog for a complete net list.

> **Please note:** The pinout of the BGA footprint does not follow IPC convention. Please triple check your footprint pin numbers against the figure below to ensure correct pinout.

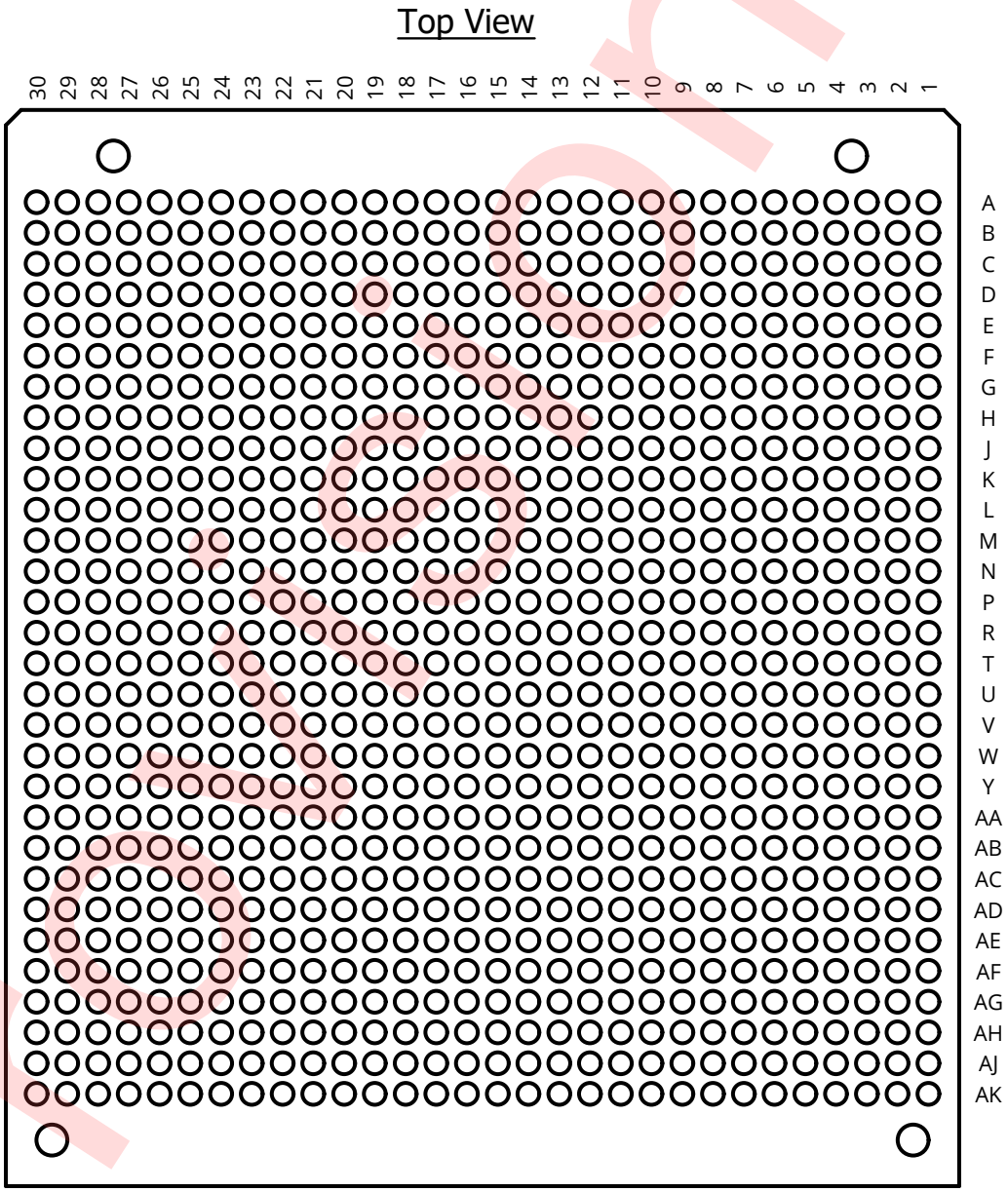


Figure 1: PactivR Pin Map

Pin Description

Please contact ProGrAnalog for a complete net list.

Table 8: Pin Description

Pin Name(s)	Pin Function
VCC_LCx	Power pins for the LoadCells
GND	Ground pins for the Pactiv
VSNS_x_P, VSNS_x_N	Voltage sense pairs
PM_SCLx	Clock for PMBus x
PM_SDAx	Data for PMBus x
PM_INTx	Interrupt/Alert for PMBus x
AVS_PWRx	Power for level translator for AVS Bus x
AVS_CLKx	Clock from Pactiv for AVS Bus x
AVS_MDATx	Data from Pactiv for AVS Bus x
AVS_SDATx	Data to Pactiv for AVS Bus x
GPIOx	3.3V logic general purpose digital I/O
NOR_PWR	Power from Pactiv to power optional flash memory
NOR_SCK	Clock from Pactiv for optional flash memory
NOR_SDA	Data to/from Pactiv for optional flash memory
UIO_PWR_y	Power to drive user I/O bank y
UIO_A_x	User I/O pins associated with bank A
UIO_B_x	User I/O pins associated with bank B

Functional Description

LoadCells

Each LoadCell can be thought of as a voltage-controlled current-sink with some minimum resistance and parasitic inductance, as shown in Figure 2. It is important to note: the voltage across the current source must remain greater than $0V$. The Orac Controller applies a voltage proportional to the current requested to the LoadCells that were configured.

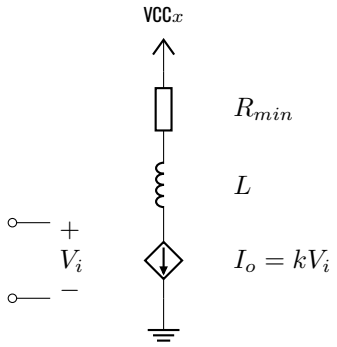


Figure 2: LoadCell Simplified Diagram

The LoadCells can be put in parallel to reduce the effects of parasitic inductance and resistances; allowing for faster edges, more current, or both.

Figure 3 shows how the LoadCell pins are distributed in the socket. Each colored area is inter-stitched with power and ground pins to provide a low impedance connection to the Device Under Test (DUT). All LoadCells share a common ground on the PactivR.

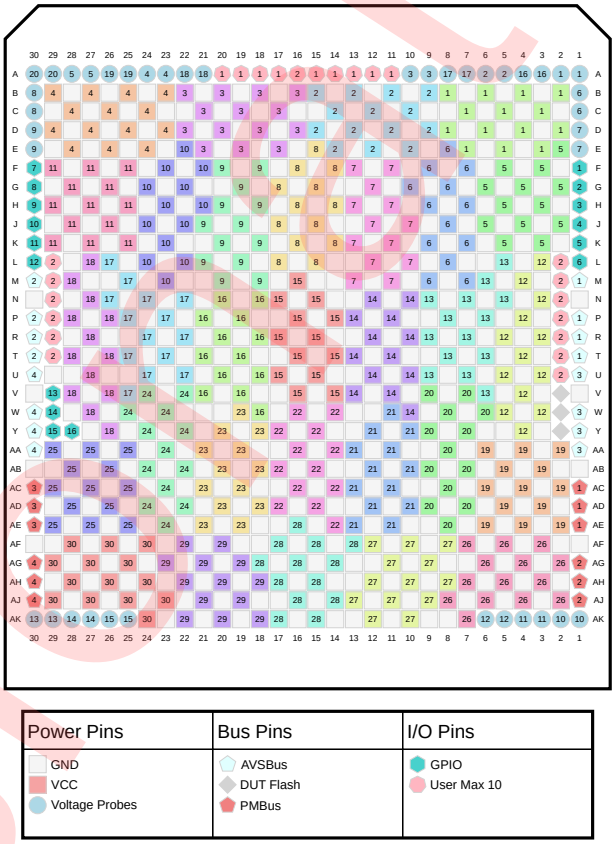


Figure 3: LoadCell Map (Top View) – Pin A1 is in the top right near LoadCell 1

User Flash Memory

The user has an option to put down a flash memory on their DUT, or on their Adapter. The flash memory identifies the Adapter/DUT to allow for the automatic configuration of the GUI.

Recommended Parts:

- M24M02-DRCS6TP/K
- M24C02-FMN6TP

PMBus

The PactivR has 4 sets of PMBus pins. They share a root PMBus controller but are separated by a mux, so each PMBus section is isolated. The DUT/Adapter is expected to pull these up to the appropriate voltage between +1.2V to +3.3V.

The Orac controller allows for the automated collection of telemetry data.

AVSBus

PactivR has 4 independent AVSBus branches. They can be used to adjust the output voltage, or gather telemetry data automatically.

GPIO

A set of 16 3.3V digital I/O is available to use. The timing on these is not precise, on the order of 1ms.

These are intended to allow the control and monitoring of system monitor type signals. Resets, enables, power goods, etc.

User FPGA

A user-programmable Max10 FPGA is included in the PactivR. In addition to the user I/O pinned-out to the socket, there is a serial bus that communicates back to the Orac Controller for control and data collection.

Differential External I/O

The External I/O, located on the top of PactivR, are 4 differential pairs that can used for output telemetry from PactivR, and 2 of those can also be used as inputs to the Orac Controller. Each external connector is also connected to a low-speed, highly-accurate ADC to perform a DC voltage meter function.

When acting as outputs, every differential pair is assignable to any available signal. Those signals are listed in Table 9.

Table 9: External I/O Output signals

Signal Name
VSNS_BUFF3
VSNS_BUFF4
WG_1A
WG_1B
WG_2A
WG_2B
ISUM_BUFF5
ISUM_BUFF6
ISUM_BUFF7
ISUM_BUFF8

When acting as inputs they are capable of ±60V.

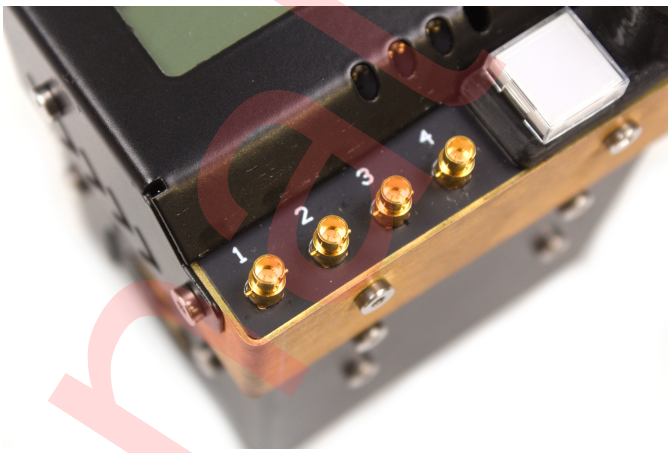


Figure 4: PactivR Differential External I/O connectors

Liquid Cooling

The PactivR comes pre-filled with Koolance 705 liquid coolant along with QDT3 quick disconnect no-spill couplings connected to 10mm x 13mm Tygon tubing. The tubing length is approximately 42 inches. One tube has the QDT3-F10X13 connector and the other has the QDT3-M10X13 connector. The flow of the coolant is not directional; either tube can be the input flow.

The PactivR unit can be shipped empty upon request, if you would like to use your own coolant. The materials coming in contact with the coolant in the loop is EPDM rubber, Tygon tubing, and nickel plated copper/brass.

We recommend the Koolance EXC-900 chiller for most customers' cooling needs. Table 10 lists the recommended items for getting started. The assembly can be done without tools.

We suggest a minimum coolant flow of 5 L/min.

Table 10: Koolance EXC-900 kit

Koolance PN	Qty
EXC-900-110V	1
FIT-L10X13	2
LIQ-705CL-05L	1
QDT3-F10X13	1
QDT3-M10X13	1
HOS-10X13PU-CL-3M	1

Figure 5: Koolance QDT3 connectors

Figure 6: PactivR with attached cooling tubes

Signal Routing

The diagram below, all signals are routed differentially to avoid both common-mode noise and negative ground effects.

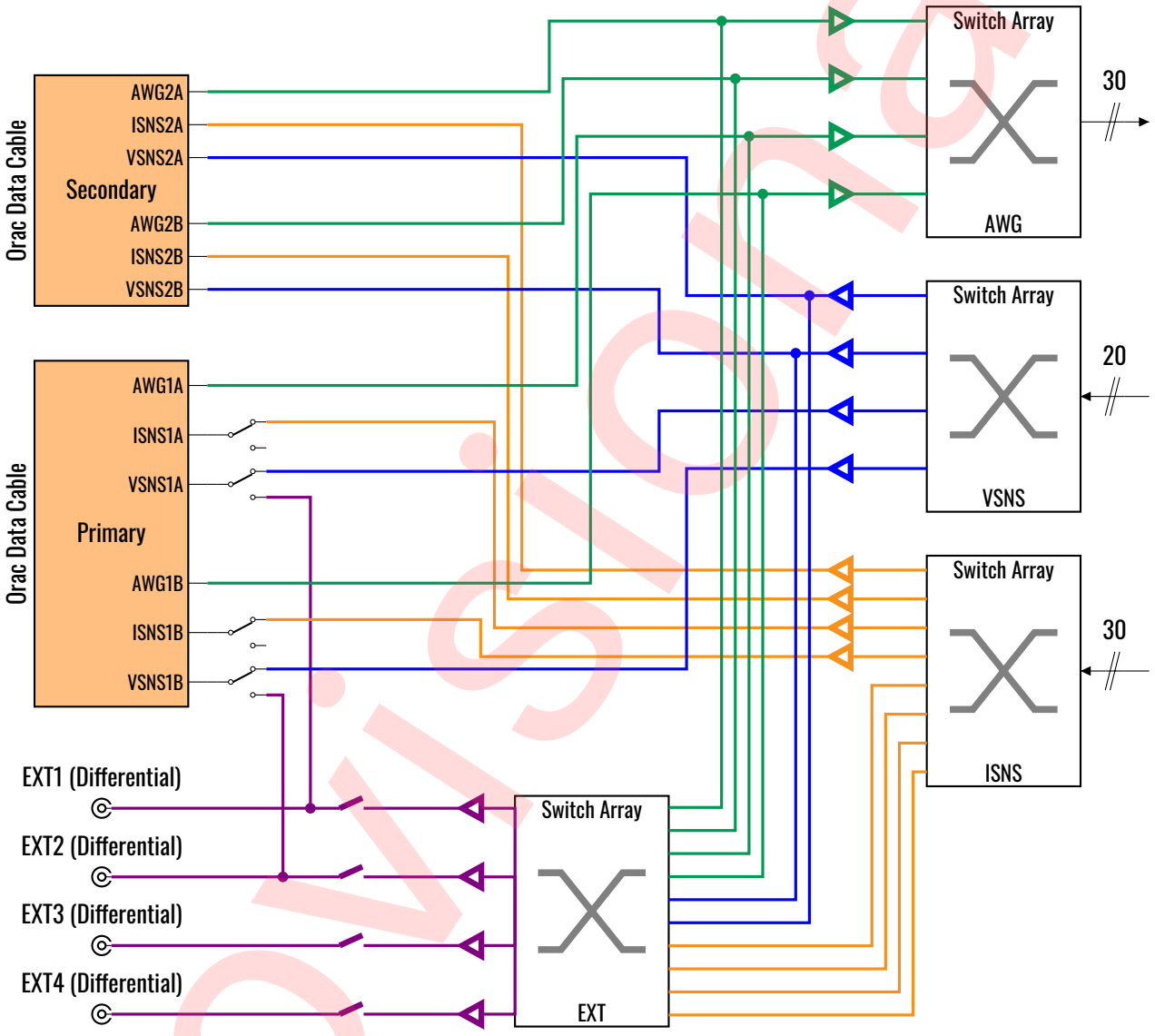


Figure 7: Simplified Signal Routing Diagram

Drawing, Dimensions, and Footprints

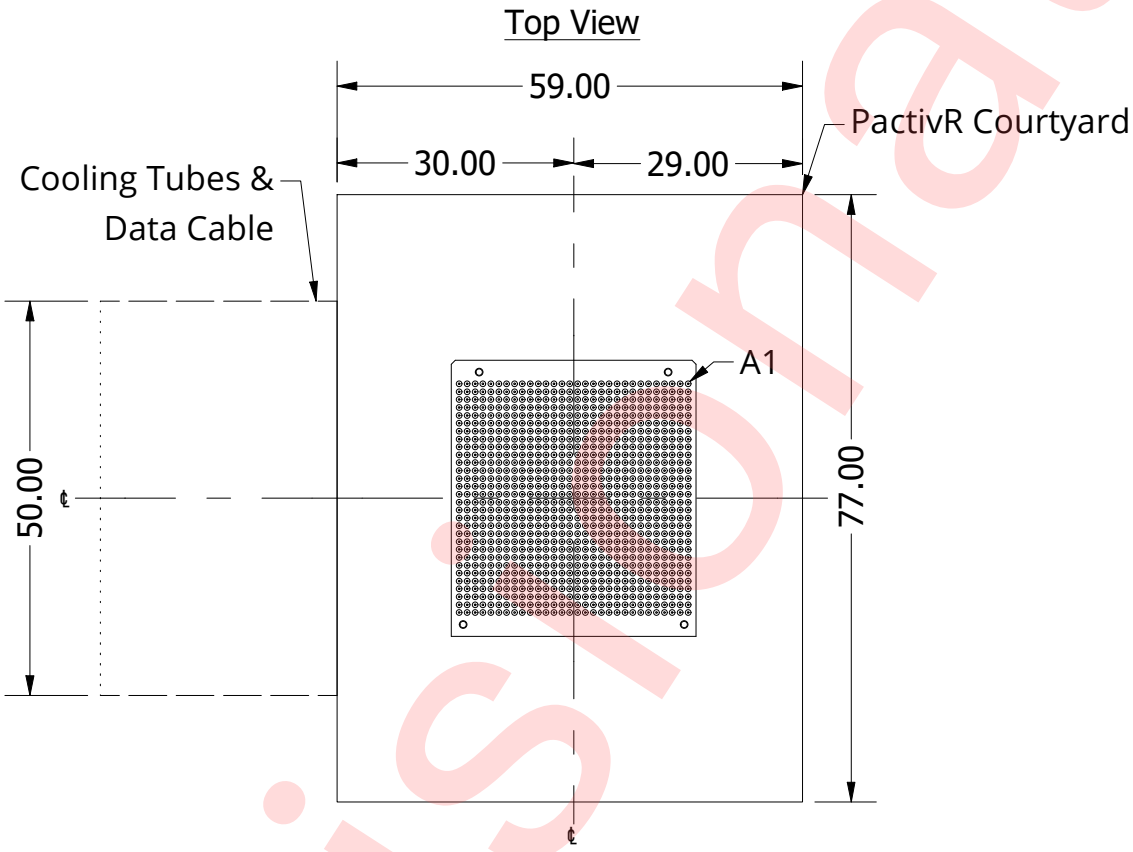
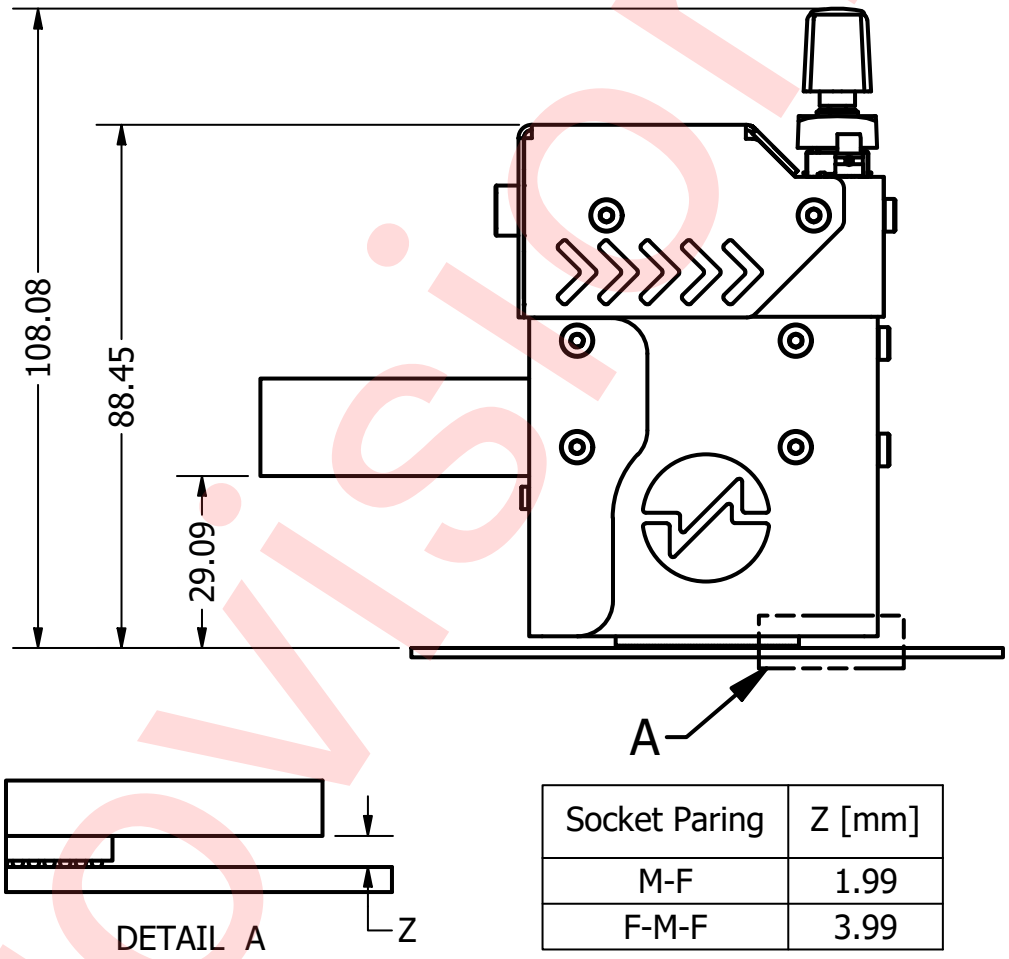


Figure 8: PactivR Keepout



Socket Paring	Z [mm]
M-F	1.99
F-M-F	3.99

Figure 9: PactivR Side Profile

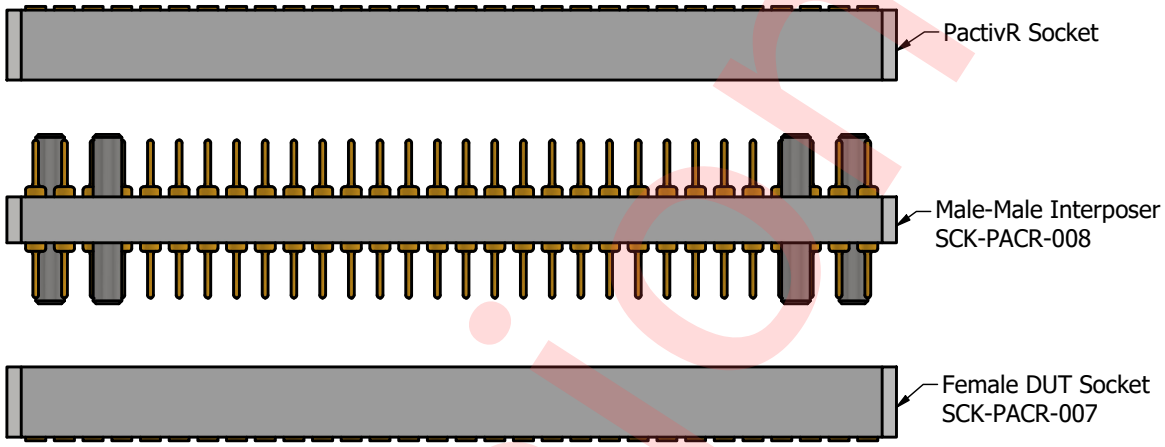


Figure 10: PactivR F-M-F Socket Side Profile

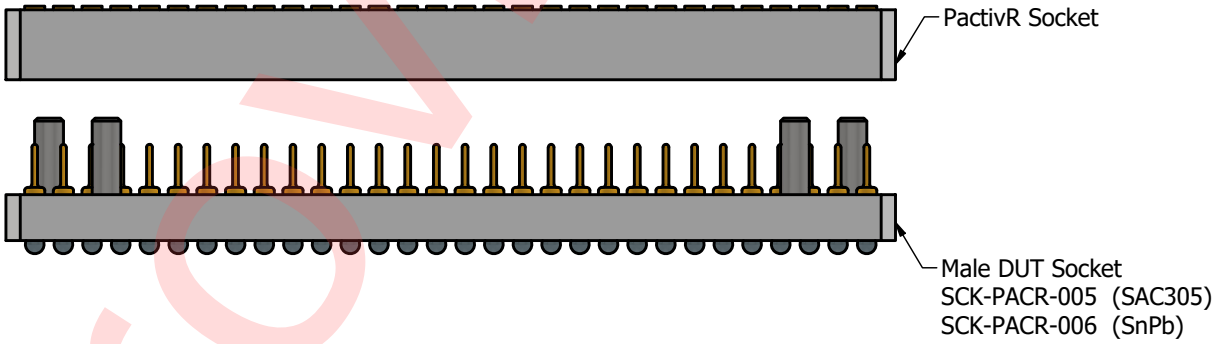


Figure 11: PactivR M-F Socket Side Profile

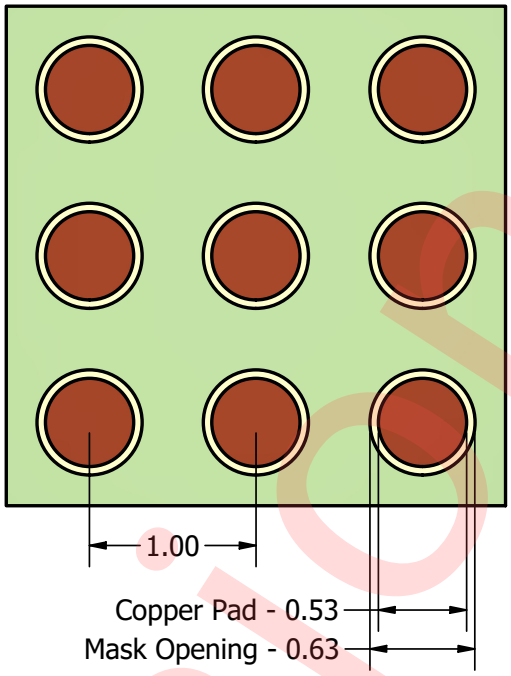
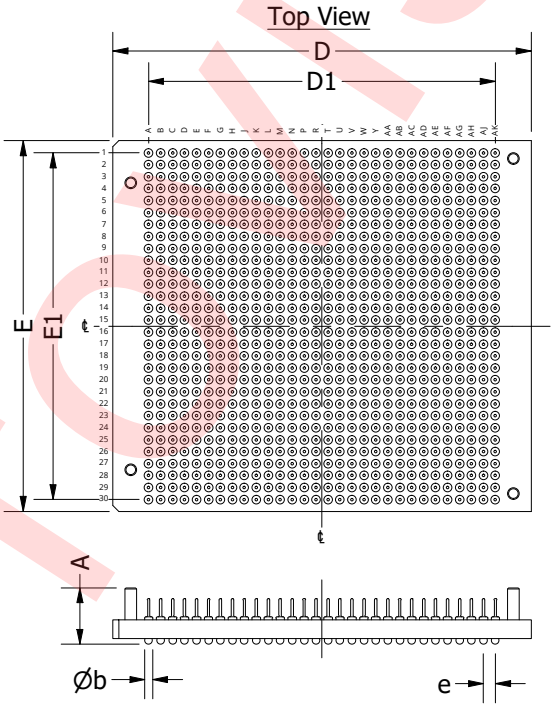
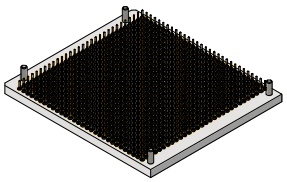


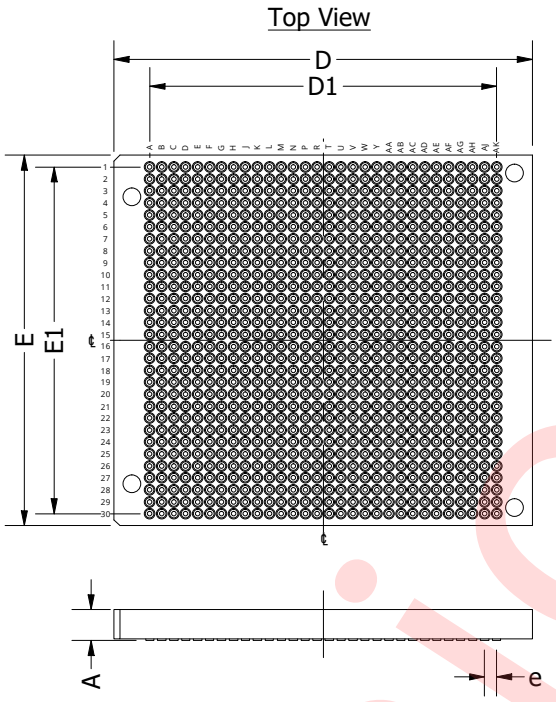
Figure 12: Footprint Recommendation – Non-Solder Mask Defined Pads

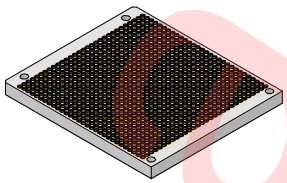




MILLIMETERS			
Symbol	MIN	NOM	MAX
A		4.73	
D		35.00	
E		31.00	
D1		29.00	
E1		29.00	
e		1.00	
Øb		0.45	
M		30	

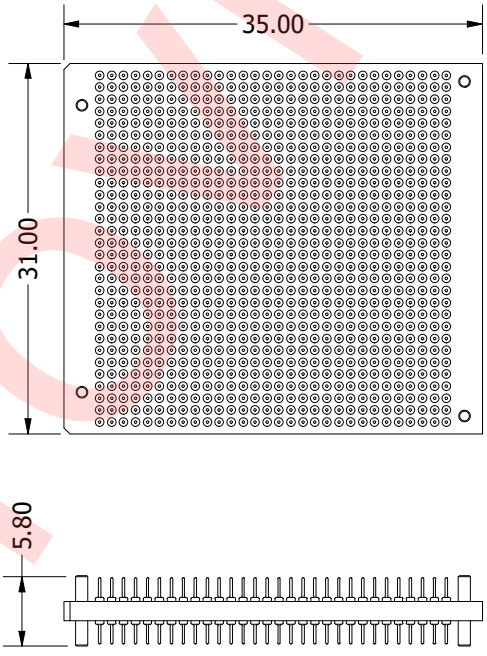
Figure 13: PactivR Male Socket Drawing - SCK-PACR-005 (SAC305), SCK-PACR-006 (SnPb)





MILLIMETERS			
Symbol	MIN	NOM	MAX
A		2.57	
D		35.00	
E		31.00	
D1		29.00	
E1		29.00	
e		1.00	
M		30	

Figure 14: Female Socket Drawing - SCK-PACR-007



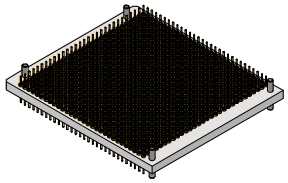


Figure 15: Male-Male Interposer Drawing - SCK-PACR-008

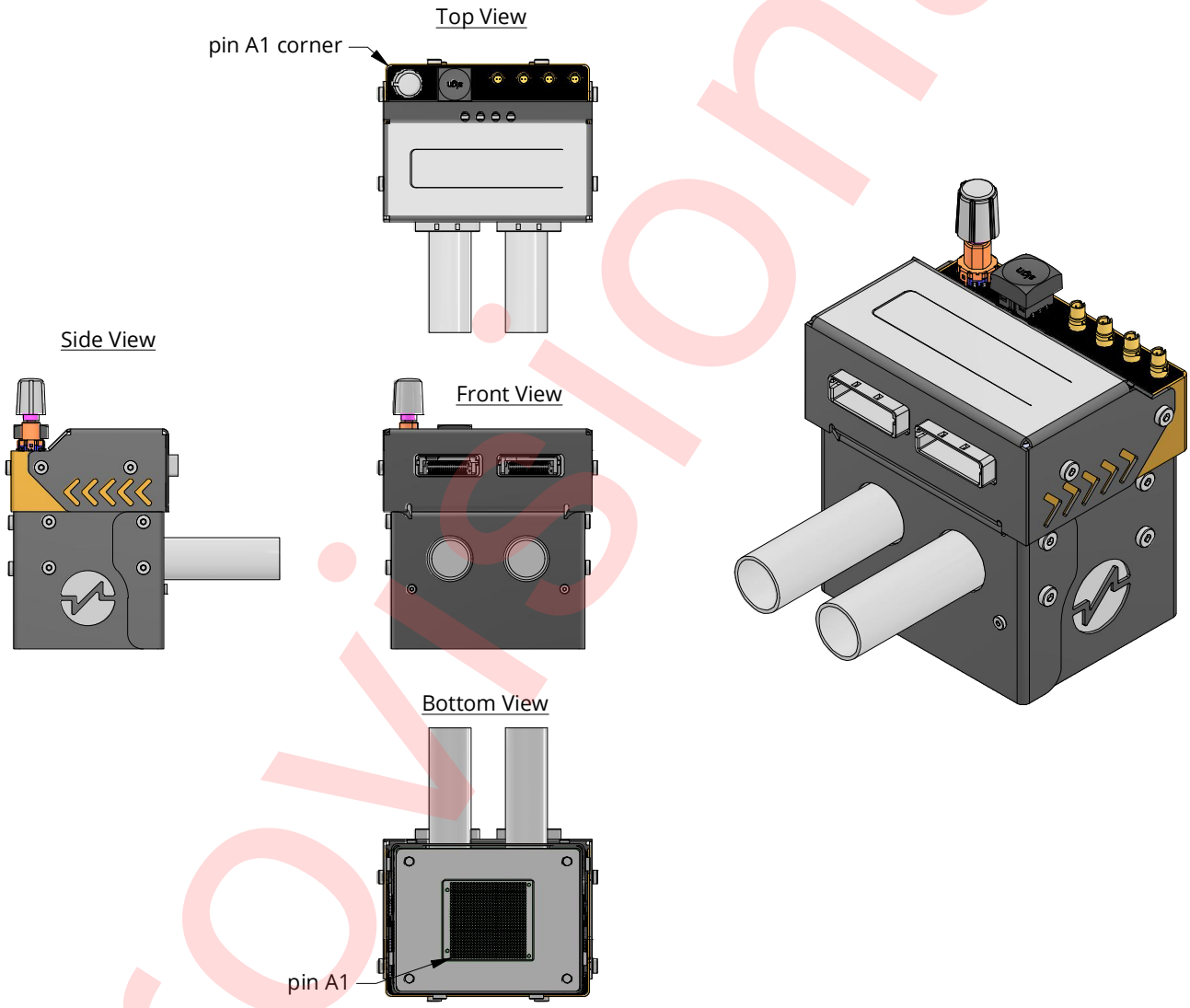


Figure 16: PactivR Drawing