LOADSLAMMER
TRUST AND VERIFY

Optimizing Regulator Output Capacitance (Part 3): Analyzing Load Slammer Results

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In this three-part series, the previous installment discussed types of load testing that can potentially be performed with load slammers.[1,2] In this last part, we show some scope plots of actual testing using a load slammer, along with commentary on what those waveforms can tell us.

After describing the voltage regulator being used in our test examples, we'll demonstrate measurements of the regulator's full step and release response, response at reduced slew rate, and output ringing. The analysis of these measurements should help to illustrate the benefits of load slammers which have been discussed throughout this series, and which are summarized at the end of this part 3. We conclude this series by explaining how slammers can help to address capacitor sourcing challenges (Appendix 1) and their value in supporting reuse of voltage regulator designs (Appendix 2).

Device Under Test And Test Setup

The voltage regulator used in these tests is a dual-phase buck regulator with an input voltage of 12 V and output voltage of 1.50 V. Operating in current mode, loop bandwidth is approximately 40 kHz with phase margin exceeding 80°. Fig. 1 shows the voltage regulator under test connected to a load slammer.

Since this board did not have a slammer connector, the slammer was directly soldered to the board with minimal connection length. Distance from the slammer to output capacitors was 10 mm or a bit more, with a 10-µF ceramic next to the slammer. Output voltage measurements were taken from the regulator board, and current measurements were taken from the slammer.

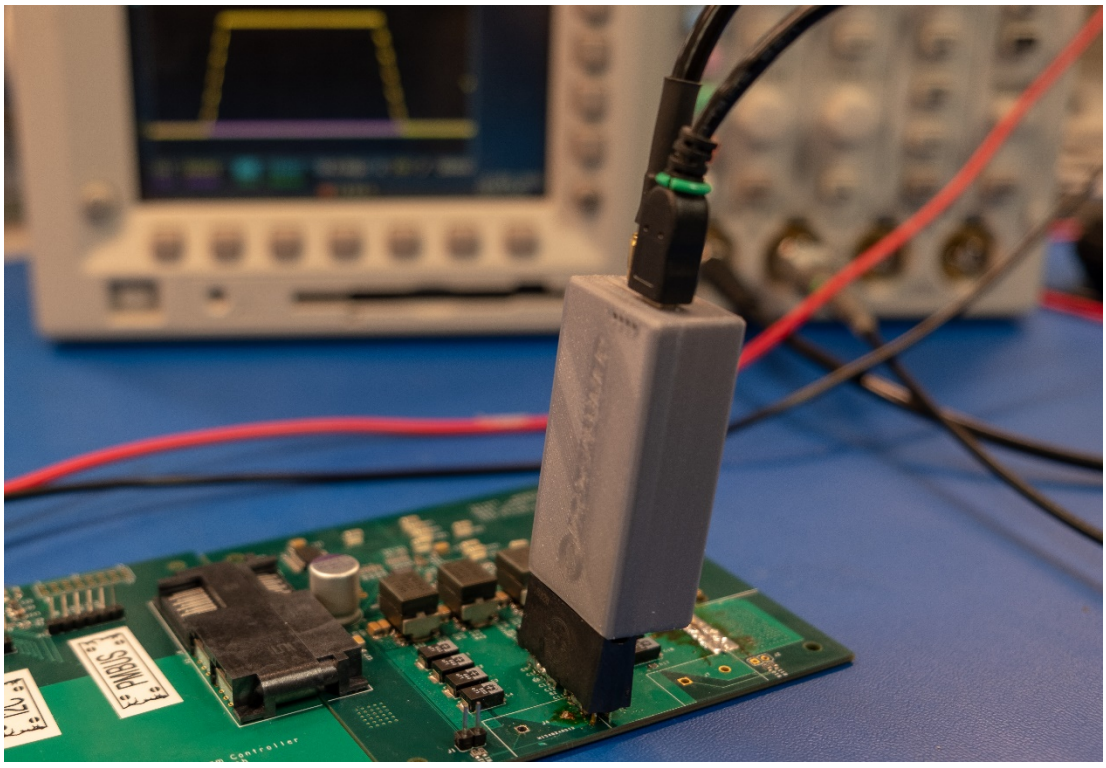

Fig 1. Slammer test setup.

Measuring Full Step And Release Response

To start transient testing, the slammer GUI was adjusted for a positive current pulse of approximately 400 µs as shown in Fig. 2. This was chosen based on the loop bandwidth of the regulator and shows a full step and release response.

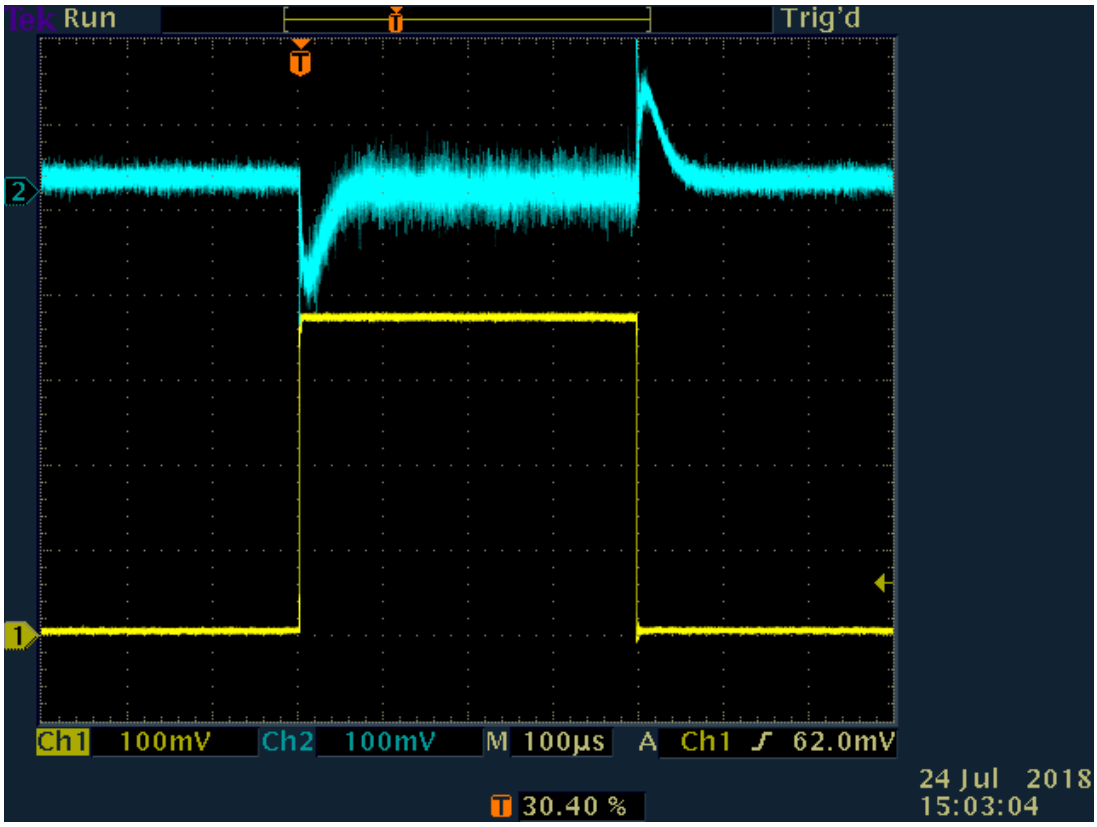

Fig. 2. Step load and release response of the voltage regulator. Initial Setting. Blue trace = Vout and yellow trace = Iout at 75 A/V.

What can we learn from this plot? Here are some thoughts:

- The current step is 0 A to 28 A, which is a reasonable value for exercising a 32-A converter.
- There is ringing on both step and release which is above the loop bandwidth. This will be related to output decoupling and will be discussed later. Averaging is used to get out some of the switching noise so that we can better see what is happening.
- The pulse is wide enough to provide time for a full response, returning to steady-state operation.
- Step and release waveforms are essentially identical, indicating that the converter response is small-signal dominant. Large-signal inductor slewing is not an issue.
- There is no ring in the loop response, which is consistent with high loop phase margin.
- The slammer current waveform is crisp and square, facilitating a clean and repeatable step response. There is little current ring and no tilting or decay as with some load units.

Fig. 3 zooms in on the initial step to see more detail.

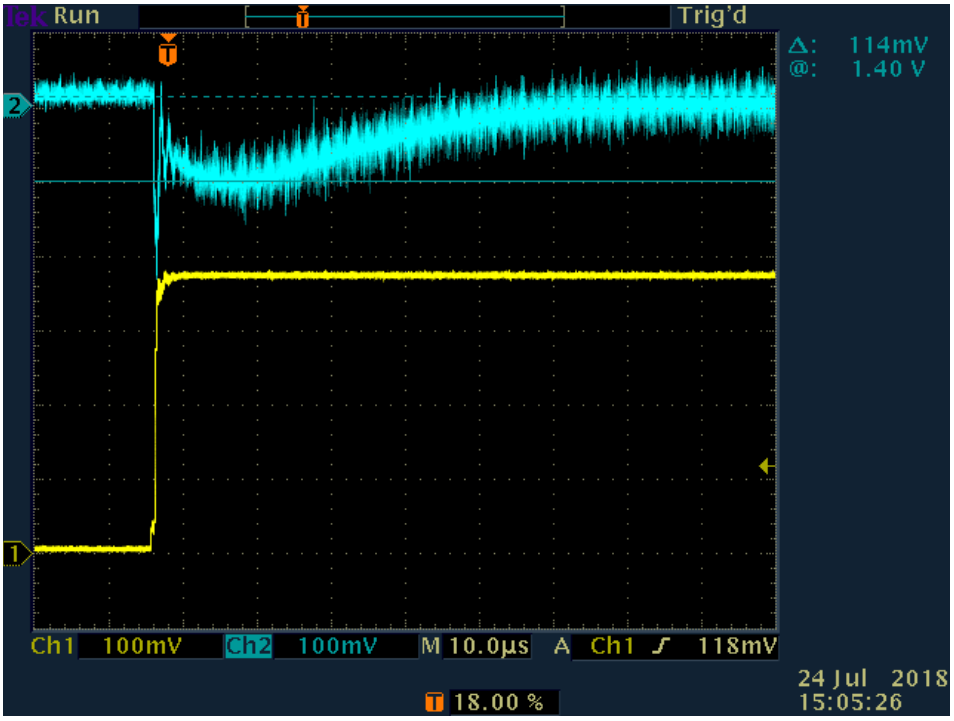

Fig. 3. 28-A Load Step for measuring undershoot. Blue trace = Vout and yellow trace = Iout at 75 A/V.

Maximum undershoot is 114 mV (7.6% under) for load step. Fig. 4 looks at response time.

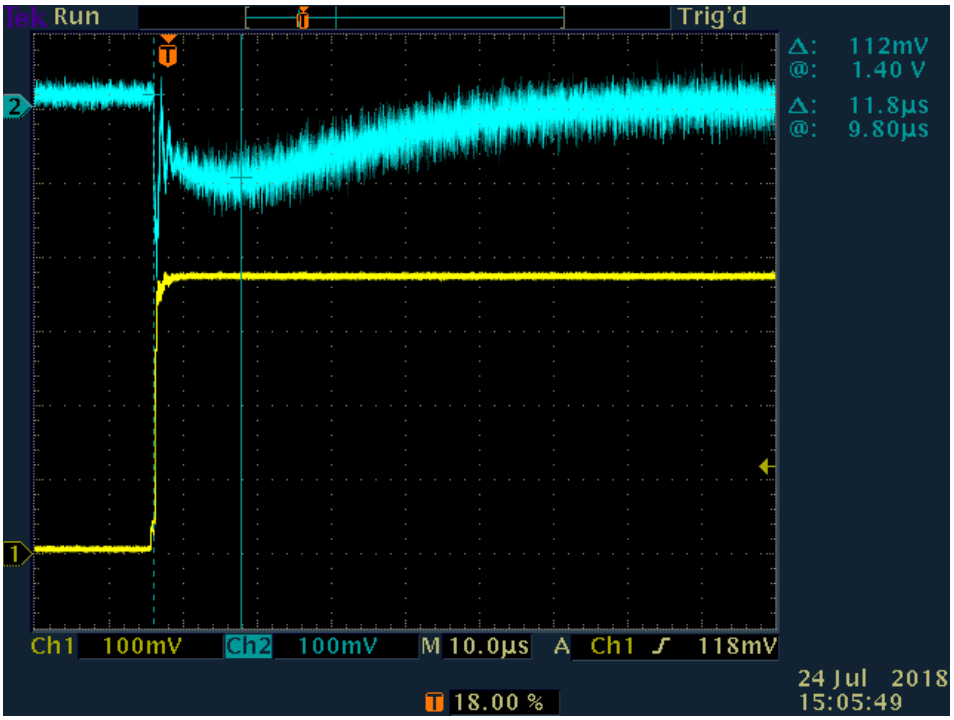

Fig. 4. Load step for measuring response time. Blue trace = Vout and yellow trace = Iout at 75 A/V.

What can we learn?

- Step response is 9.8 µs to maximum undershoot. This is about 2.2 times the loop time constant (based upon the known 40-kHz loop bandwidth).
- Recovery to steady state is roughly 50 µs later.
- Recovery time is largely dependent upon the integrating capacitor in the feedback loop. Reducing the integrating capacitor value will reduce recovery time, if phase margin is still good.

Measuring Response With Reduced Slew Rate

Next, let's discuss slew rate implementation as it relates to slammers. Fig. 5 shows a 32-A step, but with a reduced overall current slew rate, realized using discrete smaller current steps.

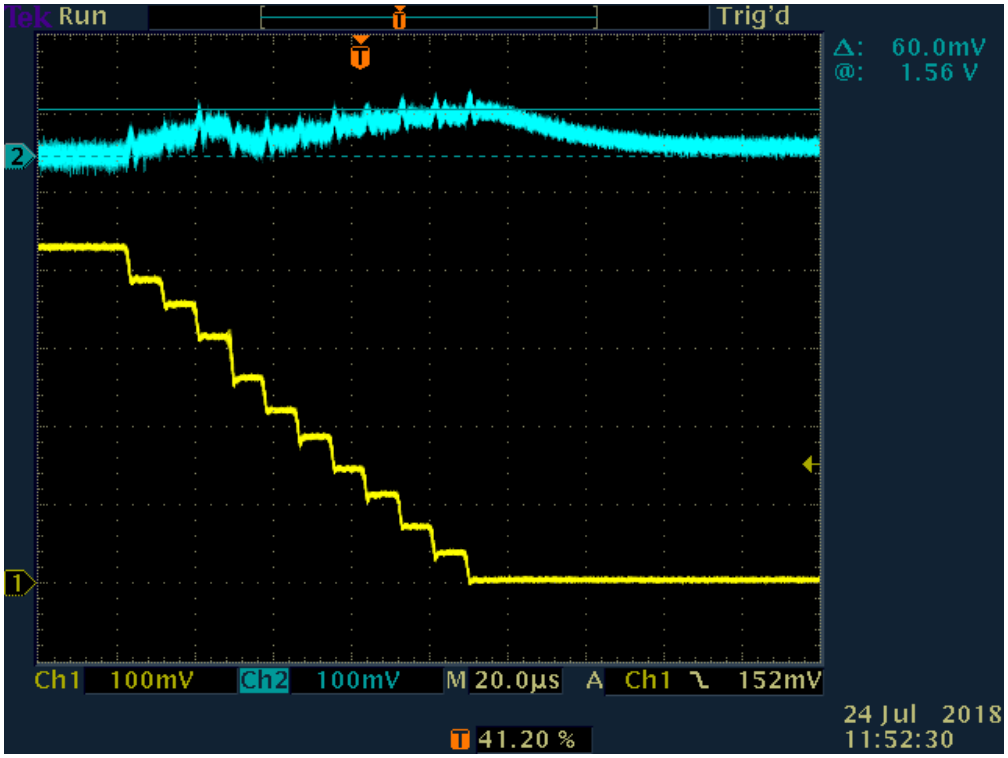

Fig. 5. 32-A stepped slew. Blue trace = Vout and yellow trace = Iout at 75 A/V.

While this method may appear coarse, it has some distinct advantages. First, it is much easier and less expensive to implement than a variable analog slewing circuit. It is also more accurate on a macro scale because the step sizes and timing are known and controlled. Another benefit is that it's easy to implement and adjust with a microcontroller via GUI and USB interface.

Using this method to slow the current slew rate allows us to learn more about the how slew rate affects transient response.

- 32 A is stepped in approximately 88 µs, for a slew rate of 0.36 A/µs.
- Liftoff is only 60 mV (4.0% over), which is much lower than our previous 28-A response. Why the difference?
- The slower di/dt allows the regulator loop to respond as the step is slewing. Conversely, if load slew rate requirements are low, it is easier and potentially less expensive to design a regulator that can meet those requirements.
- This demonstrates the usefulness of having a variable slew rate.

A Closer Look At Ringing

Lastly, let's discuss the ring seen in earlier scope plots and how it relates to load-current slew rate. As seen above, the variable rate is accomplished with a series of smaller steps getting ever closer together. When the steps narrow sufficiently, they begin to disappear, and the waveform becomes analog. Ringing occurs due to parasitic circuit elements, both in the slammer and the load. Fig. 6 shows a load step of roughly 93 A/µs.

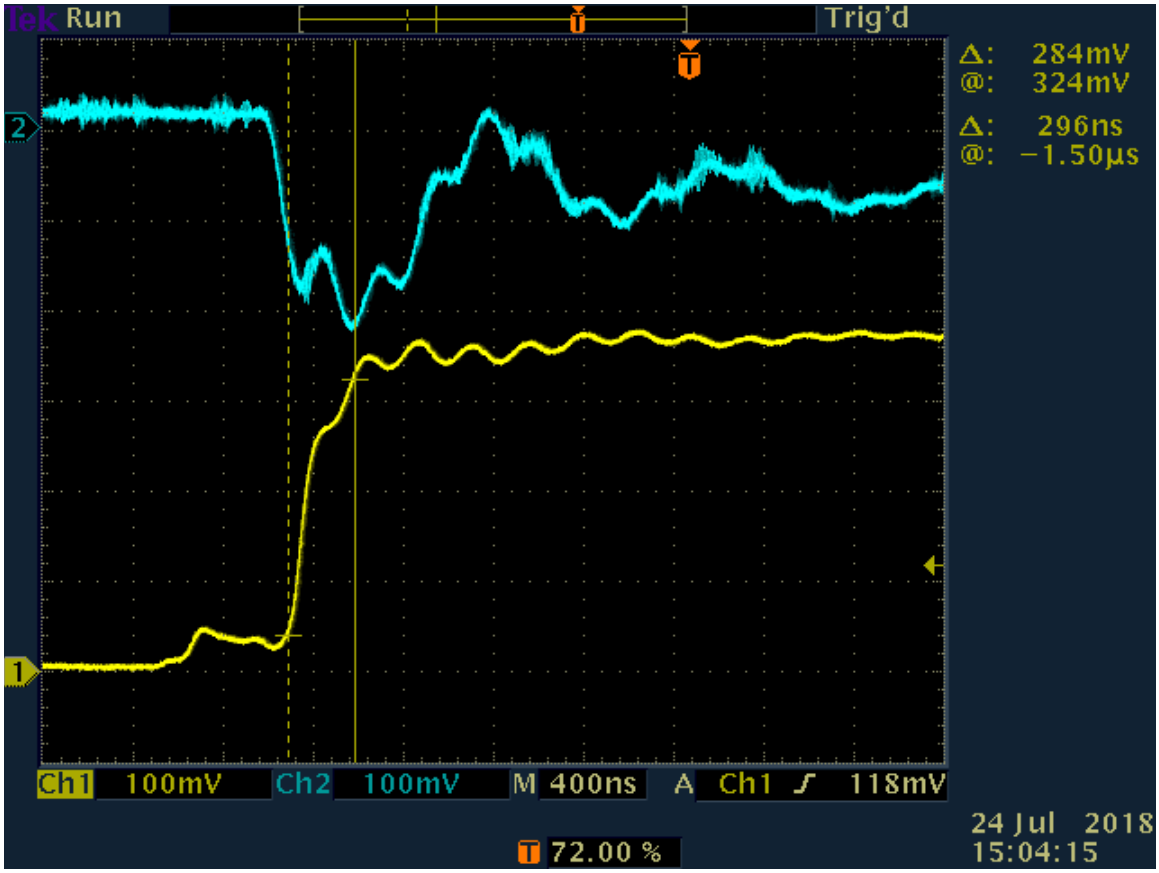

Fig. 6. 93-A/us load step. Blue trace = Vout and yellow trace = Iout at 75 A/V.

At this rate, we are well beyond the loop and looking at the output decoupling solution of the voltage regulator. Output voltage deviation is 240 mV.

Fig. 7 shows a load release slew rate of 55 A/us. Output voltage deviation, off the screen in this picture, is about 300 mV.

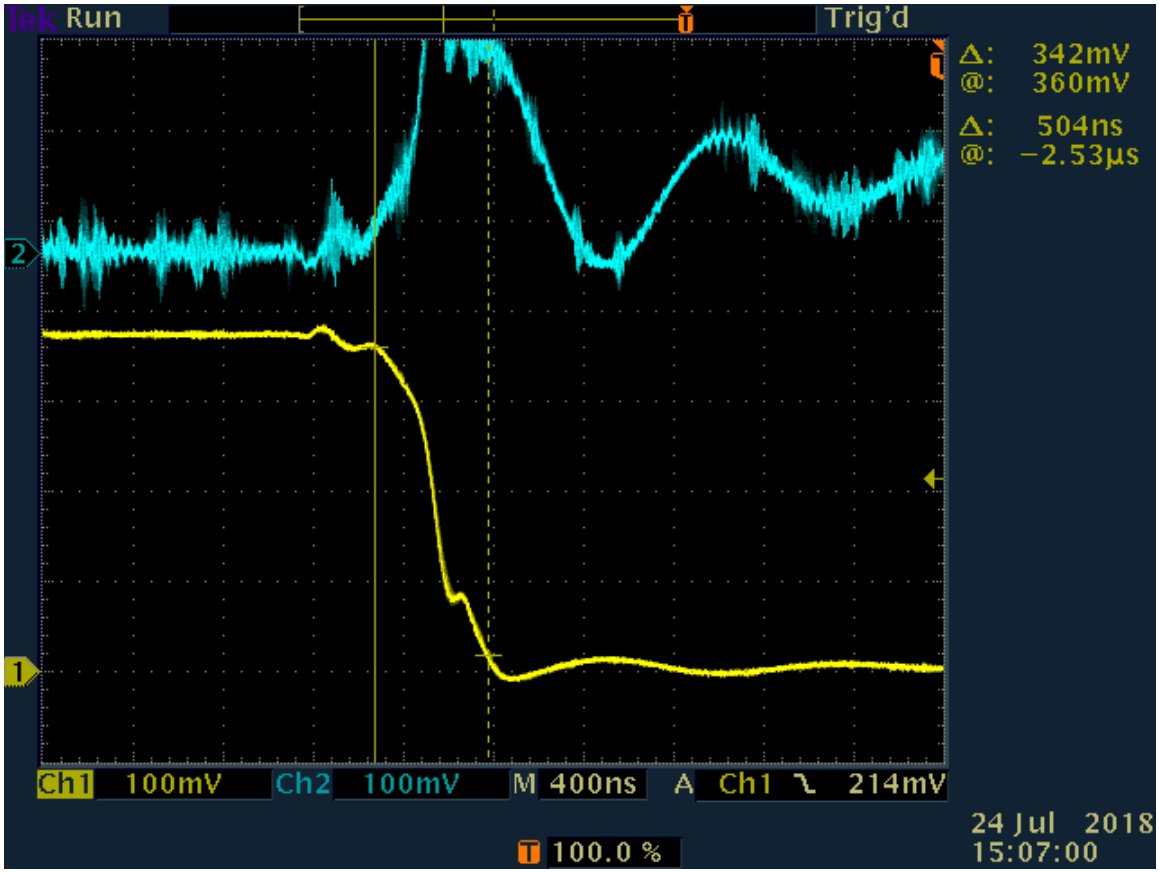

Fig. 7. 55-A/us load release. Blue trace = Vout and yellow trace = Iout at 75 A/V.

Here are some final observations on this measurement:

- Output voltage rings at around 830 kHz on both step and release. This would calculate to the 10-µF ceramic ringing with 3.7 nH of inductance. This is very possible given the board trace length to output bulk capacitors and the ESL (equivalent series inductance) of the polymer output capacitors.
- There is an additional ring on the step edge of approximately 4.5 MHz, possibly due to the faster edge in the step waveform.
- There is no input capacitance on the slammer other than parasitic MOSFET capacitance. This allows extremely fast response but it can also ring, depending on the regulator output impedance. Care should be taken to minimize the distance between the slammer and voltage regulator output decoupling.
- A more complete regulator output filter solution (more ceramic capacitors near the output or shorter traces) will likely reduce output voltage deviation and ringing. Thus, the slammer can supply useful information well above the loop bandwidth.

Conclusion

Load slammers are low-cost, affordable instruments, in contrast with expensive, calibrated, full-featured load systems. As this series has demonstrated, they are an effective tool in measuring transient response of board-level converters. They corroborate testing with other instruments (such as Bode analyzers) and with simulation.

Load slammers can also provide some level of loop information independently. The latter includes response time (related to loop bandwidth), recovery time (related to integrating capacitor value) and very approximate phase margin.

Slammers can help distinguish between small-signal dominant and large-signal dominant responses. They can also exercise a voltage regulator consistently and repeatably. Step size can start small and benign, increasing to beyond what the actual load may require. This helps test for margin in design.

Variable current slew rates show how regulator response can vary, depending upon load requirements, aiding in optimizing regulator design. Very fast slew rates can provide useful information regarding the regulator output decoupling solution.

It is my sincere hope that you find this article series helpful for your design and testing efforts. Don't be afraid to experiment and probe to learn more about your voltage regulator—its good points, bad points, transitions, and limits.

Now have fun and go slam some loads!

Appendix 1: Load Slammers Save Your Bacon

One major issue currently facing manufacturers is difficulty in procuring components, especially multilayer ceramic capacitors (MLCCs). There are two primary reasons for this situation. One is that the market for components is way up, increasing costs and stretching lead times. Many parts are hard to obtain at all. Another reason is that many manufacturers are trending toward smaller package sizes—0402 and smaller. This leaves fewer vendors with larger-sized MLCCs.

How can slammers help?

Through optimizing your regulator loop. Assuming equal phase margins, doubling the bandwidth of the loop can halve output capacitor requirements. This not only saves money, but fewer capacitors are easier to source. Alternately, the same number of 0402 MLCCs may suffice instead of 0603 packages.

A third option would be to tilt toward aluminum or polymer bulk capacitors with ceramic high-frequency bypass. Yet another option would be to increase operating frequency, requiring less output filtering and increasing potential loop bandwidth. All verified by a load slammer.

Appendix 2: Load Slammers To The Rescue… (Cue Jim Dandy)

Have you ever borrowed a regulator circuit design and placed it on your board without thinking? There are manifold reasons to reuse part numbers and circuits, and not reinvent the wheel. Not that any of us are ever pushed for time.

Yet, what exactly were the assumptions for the first application? Many designs start clean, but like the telephone game, successive iterations can deviate from the original intent. Or, new applications have different requirements which the original circuit was never meant to address. What to do when the loop flies the coop?

Debugging can get even more interesting trying to create an injection point for a Bode analyzer, when feedback runs are buried deep in a multilayer board.

Enter the load slammer. There is almost always a place to connect because output filter components are nearly always accessible. When dealing with existing boards, a combination of loop calculations, simulation, and slammers can often save the day. And your sanity.

References

1. "Optimizing Regulator Output Capacitance (Part 1): Selecting Load Slammers" by David Baretich, Hpw2Power Today, August 2018 issue.

2. "Optimizing Regulator Output Capacitance (Part 2): Using Load Slammers" by David Baretich, How2Power Today, September 2018 issue.

3. "Removing Capacitors With Load Slammer," YouTube video, October 2, 2018.

About The Author

David Baretich is an electrical engineer and consultant to ProGrAnalog. He has 38 years' experience in power conversion, working at companies such as Texas Instruments, MicroPlanet, ON Semiconductor, Tektronix and Biamp Systems. An IEEE member, David holds 10 U.S. patents. He received a BSEE from Iowa State University.